REMARKS/ARGUMENTS

Claims 14-17 are pending in the application. By this amendment, claim 14 is being amended to improve its form. No new matter is involved.

In paragraph 3 which begins on page 2 of the Office Action, claims 14-17 are rejected under 35 U.S.C. § 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over, U.S. Patent 5,447,890 of Kato et al. According to the Office Action, Kato describes a method in accordance with most of the limitations of the claims, but does not explicitly teach the limitations of the wafer having undulation components on the wafer back surface of 10 μm^3 or less represented in terms of power spectrum density at least for the components at a wavelength of 10 mm and/or a variation of power spectrum density of 2.0 or less for undulation components at a wavelength of from 3 mm to 20 mm of the wafer back surface. According to the Office Action, however, it is reasonable to presume that such limitations are inherent to the invention. Support for this is said to be found in the use of similar materials, and the burden is said to be upon applicant to prove otherwise. Further, and in the alternative, Kato's method is said to describe the reversed surface-polishing step in order to remove undulations or irregularities, on the reversed side of the wafer before the polishing of the observed surface, so that it would have been obvious to one of skill in the art by Kato's teaching that it is desired to have less irregularity in the back surface. These rejections are respectfully traversed.

Claim 14 is being amended in order to more clearly distinguish patentably over the art. As amended, the claim defines a method for producing a semiconductor wafer by polishing a surface of the semiconductor wafer which is held at its back surface, which determines a back surface profile and analyzes its frequency "to calculate its power spectrum density" at least before holding the semiconductor wafer. This is in accordance with lines 10-14 of page 14 of the

specification where calculation of the power spectrum density is described. Similarly, line 7 of page 15 also describes calculation of the power spectrum density. As so amended, claim14 also recites "and polishes only a semiconductor wafer having undulation components on wafer backed surface (emphasis added)". This is in accordance with the description at lines 9-16 of page 21, and particularly line 13 which refers to "only those wafers having undulation components".

As amended herein, claim 14 reads as follows:

14. A method for producing a semiconductor wafer by polishing a surface of the semiconductor wafer which is held at its back surface, which determines a back surface profile and analyzes its frequency to calculate its power spectrum density at least before holding the semiconductor wafer, and polishes only a semiconductor wafer having undulation components on wafer back surface of 10 μm^3 or less represented in terms of power spectrum density at least for the components at a wavelength of 10 mm and/or a variation of power spectrum density at 2.0 or less for undulation components at a wavelength of from 3 mm to 20 mm of the wafer back surface.

Thus, claim 14 characterizes the method for producing a semiconductor wafer in accordance with the invention in terms of the power spectrum density (hereinafter PSD) of the semiconductor wafer being calculated at least before holding the semiconductor wafer, a semiconductor wafer having undulation components on wafer back surface of 10 μm^3 or less represented in terms of PSD at least for the components at a wavelength of 10 mm and/or a variation of PSD of 2.0 or less for undulation components at a wavelength of from 3 mm to 20 mm of the wafer back surface is selected, and only a semiconductor wafer having undulation components of such a range is polished.

Therefore, and in accordance with the present invention, by calculating PSD of the semiconductor wafer as described above, undulation components of

semiconductor wafers can be quantitatively evaluated, as described in lines 23-25 of page 9 of the specification. And if undulation components of semiconductor wafers can be quantitatively evaluated in this manner, a semiconductor wafer having undulation components (that is, the value of PSD and/or variation of PSD) as described above is selected, and only a selected wafer can be polished. And thereby, and as described beginning with the 3rd line from the bottom of page 20 through line 8 of page 21 of the specification, the undulations are not transferred to the front surface in polishing because the back surface to be held does not have undulations, and thus a semiconductor wafer having a good surface profile can be produced.

On the other hand, and as asserted in the last five lines of page 2 and the first line at the top of page 3 of the Office Action, Kato describes that in the reverse surface-preparing step E, the surface W3 vested with a roughness having an amply shorter period than the undulation W1 (in the approximate range of 1 to 10 μm, for example) and a P-V value in the approximate range of 0.1 to 0.5 μm is formed on the reverse surface of the wafer W (see line 65 of column 4 through line 6 of column 5 of Kato). It is also asserted in the Office Action that lines 17-24 of column 5 of Kato describe that the wafer which has the shape of the reverse surface thereof prepared by the reverse surface-preparing step E mentioned above, is subjected to the next obverse surface-polishing step F to have the obverse surface thereof polished and made to acquire a mirror finish. Accordingly, the Examiner asserts that this shows that the back surface profile and its frequency have to be determined or analyzed, before polishing the observed surface.

However, unlike the present invention, Kato does not calculate a power spectrum density at least before holding a semiconductor wafer, and does not polish only a semiconductor wafer having undulation components on the wafer backed surface of 10 μm^3 or less represented in terms of power spectrum density at least for the components at a wavelength of 10 mm and/or a variation of power spectrum

density of 2.0 or less for undulation components at a wavelength of from 3mm to 20mm of the wafer back surface.

In short, because Kato shows a period of an undulation and a P-V value of a wafer after the reverse surface-preparing step E, Kato may determine a back surface profile of a wafer as asserted by the Examiner. However, Kato does not calculate PSD of a semiconductor wafer before holding the semiconductor wafer, unlike the present invention. Inherently, Kato has no description of PSD or consideration about PSD in the semiconductor wafer. Also, the Office Action admits that Kato does not teach PSD (see lines 4-8 of page 3 of the Office Action). Because Kato does not calculate PSD of a semiconductor wafer, as described above, Kato cannot quantitatively evaluate undulation components of semiconductor wafers, in the manner of the present invention.

Moreover, because Kato cannot quantitatively evaluate undulation components of semiconductor wafers, as described above, it is impossible to select a semiconductor wafer having undulation components on the wafer back surface of 10 μm^3 or less represented in terms of power spectrum density at least for the components at a wavelength of 10 mm and/or a variation of power spectrum density of 2.0 or less for undulation components at a wavelength of from 3 mm to 20 mm of the wafer back surface. Accordingly, it is impossible to polish only a semiconductor wafer having undulation components of such a range, as in the case of the present invention.

Additionally, it is asserted in the Office Action that it is reasonable to presume that such limitations are inherent to the invention of Kato (see lines 8-9 of page 3 of the Office Action).

To the contrary, however, the undulation components of the wafer vary significantly, depending on the wafer production conditions and the like, as clearly exemplified in the examples, in Fig. 2 and in other places of the present

specification. Therefore, unless the PSD of the wafer described in Kato is actually calculated, it cannot be determined whether the wafer has undulation components of the above range in the manner of the present invention. In short, because Kato has no description of PSD, it is impossible to select wafers as in the case of the present invention.

Because Kato does not calculate a power spectrum density of a semiconductor wafer and cannot polish only a semiconductor wafer having undulation components on wafer back surface of 10 μm^3 or less represented in terms of power spectrum density at least for the components at a wavelength of 10 mm and/or a variation of power spectrum density of 2.0 or less for undulation components at a wavelength of from 3 mm to 20 mm of the wafer back surface, Kato is different from the present invention as defined in claim 14, in terms of such features. Consequently, claim 14 is submitted to clearly distinguish patentably over Kato.

Moreover, Kato neither describes nor suggests that a power spectrum density of a semiconductor wafer is calculated, and only a semiconductor wafer having undulation components on wafer back surface of 10 μm^3 or less represented in terms of PSD at least for the components at a wavelength of 10 mm and/or a variation of PSD of 2.0 or less for undulation components at a wavelength of from 3 mm to 20 mm of the wafer back surface is polished. Therefore, even one of ordinary skill in the art would never derive the present invention as it is defined in claim 14.

And because claim 14 includes the feature that the PSD of the semiconductor wafer is calculated at least before holding the semiconductor wafer, a semiconductor wafer having undulation components on wafer back surface of 10 μm^3 or less represented in terms of PSD at least for the components at a wavelength of 10 mm and/or a variation of PSD of 2.0 or less for undulation components at a wavelength of from 3 mm to 20 mm of the wafer back surface is selected, and only such a semiconductor wafer is polished. Claim 14 provides the desirable effect that a

semiconductor wafer having a good surface profile can be produced without transferring undulations to the front surface by polishing. Again, claim 14 is submitted to clearly distinguish patentably over the art.

Claims 15-17 depend, directly or indirectly, from claim 14 and contain all of the limitations of claim 14. Therefore, claim 15-17 are also submitted to clearly distinguish patentably over the art.

In conclusion, claims 14-17 are submitted to clearly distinguish patentably over the prior art for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

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By: Lawrence J. McClure

Lawrence J. McClure
Registration No. 44,228
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-670